In the claims:

All of the claims standing for examination are reproduced below with appropriate status indication.

1-31. (Canceled)

32. (New) A semiconductor package assembly, comprising:

a die having electrical contact pads for external connection and a height; and

a predominantly metal substrate having a recessed area with a depth at least equal to the height of the die;

wherein the substrate comprises a dielectric layer on the recessed side insulating patterned circuitry extending into the recessed area, the die mounted in the recessed area with electrical connections provided between the electrical contact pads of the die and the patterned circuitry in the recessed area.

33. (New) The semiconductor package assembly of claim 32 wherein the die is mounted to the substrate circuitry, hence to the substrate, by solder balls between the electrical contact pads of the die and the patterned circuitry on the substrate in the recessed area.

34. (New) The semiconductor package assembly of claim 33 further comprising solder balls mounted to individual traces of the substrate patterned circuitry in area outside the recessed area providing facility to connect the traces to circuitry on a printed circuit board.

35. (New) The semiconductor package assembly of claim 33 further comprising vias through the dielectric layer separating the metal substrate from the patterned circuitry, and a plurality of solder ball connections to the metal of the substrate from individual ones of

the contact pads of the die, providing direct, conductive heat transfer between the die and the metal of the substrate.

36. (New) The semiconductor package assembly of claim 32 wherein the metal of the predominantly metal substrate is predominantly copper or stainless steel.

37. (New) The semiconductor package assembly of claim 32 wherein the die is mounted to the substrate in the recessed area by adhesive with the electrical contact pads facing away from the substrate, and the electrical connections are provided between the electrical contact pads of the die and the patterned circuitry in the recessed area by wire bonds.

38. (New) The semiconductor package assembly of claim 37 further comprising plastic material encapsulating the die and the wire bonds, and either package pins or solder balls connected to individual traces of the substrate patterned circuitry in substrate area outside the recessed area.

39. (New) A method for packaging a semiconductor die having electrical contact pads and a height, for coupling the die to circuitry of a printed circuit board, comprising steps of:

(a) forming a recessed area in a predominantly metal substrate, the recessed area having a depth at least equal to the height of a semiconductor die to be mounted in the recessed area;

(b) patterning circuitry on the substrate on the recessed side, both in the recessed area and in area outside the recessed area, the circuitry electrically insulated from the metal of the substrate by a dielectric layer;

(c) mounting the semiconductor die in the recessed area; and

(d) connecting individual ones of the electrical contact pads of the semiconductor die to the patterned substrate circuitry in the recessed area.

40. (New) The method of claim 39 wherein in steps (c) and (d) the die is mounted to the substrate circuitry, hence to the substrate, by solder balls between the electrical contact pads of the die and the patterned circuitry on the substrate in the recessed area.

41. (New) The method of claim 40 further comprising a step: mounting solder balls to individual traces of the substrate patterned circuitry in the area outside the recessed area providing facility to connect the traces to circuitry on a printed circuit board.

42. (New) The method of claim 40 further comprising further steps: forming vias through the dielectric layer separating the metal substrate from the patterned circuitry, and forming a plurality of solder ball connections to the metal of the substrate from individual ones of the contact pads of the die, providing direct, conductive heat transfer between the die and the metal of the substrate.

43. (New) The method of claim 39 wherein the metal of the predominantly metal substrate is predominantly copper or stainless steel.

44. (New) The method of claim 39 wherein the die is mounted to the substrate in the recessed area by adhesive with the electrical contact pads facing away from the substrate, and the electrical connections are provided between the electrical contact pads of the die and the patterned circuitry in the recessed area by wire bonds.

45. (New) The method of claim 44 further comprising steps; encapsulating the die and the wire bonds with a plastic material, and connecting either package pins or solder balls to individual traces of the substrate patterned circuitry in substrate area outside the recessed area.

46. (New) A substrate for a semiconductor package, comprising:

a metal plate having a central recessed area;

a dielectric layer formed on the metal plate on the recessed side;

patterned, electrically-conductive circuitry formed on the dielectric layer, electrically insulated from the metal plate, the circuitry extending into the recessed area.

47. (New) The substrate of claim 46 further comprising vias formed through the dielectric layer, providing direct, heat-conducting paths from the circuitry side of the substrate to the metal plate.

48. (New) The substrate of claim 46 further comprising either contact pins or solder balls mounted to the patterned, electrically-conductive circuitry in the area outside the recessed area

49. (New) A method for forming a semiconductor package substrate, comprising steps of:

(a) forming a central recessed area in metal plate;

(b) applying a dielectric layer on the metal plate on the recessed side; and

(c) forming patterned, electrically-conductive circuitry on the dielectric layer, electrically insulated from the metal plate, the circuitry extending into the recessed area.

50. (New) The method of claim 49 further comprising a step: forming vias through the dielectric layer, providing direct, heat-conducting paths from the circuitry side of the substrate to the metal plate.

51. (New) The method of claim 49 further comprising a step: mounting either contact pins or solder balls to the patterned, electrically-conductive circuitry in the area outside the recessed area.